A 5 µm Pitch VGA Resolution GeSi Lock-in Pixel Array in Backside Illumination Configuration

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***Abstract*—We demonstrate a 5 µm pitch VGA resolution GeSi lock-in pixel array in backside illumination (BSI) configuration for indirect time-of-flight (iTOF) applications. Our work paves the route to low-cost SWIR 2D/3D imagers with CMOS compatible process and possible adoption of SWIR eye-safe lasers.**

Keywords—GeSi, lock-in pixel, iTOF, SWIR, 3D imager

I. Introduction

3D image sensors based on TOF techniques have made substantial progress in recent years. In particular, for indirect TOF applications, Si lock-in pixel pitches ranging between 10 µm and 2.8 µm have been achieved to enable higher resolution [1-3]. In contrast to Si lock-in pixel, GeSi lock-in pixel was previously proposed and demonstrated with high quantum efficiency and large bandwidth using a 10 µm pitch pixel [5,6]. In this paper, we report experimental data on the pitch scaling of GeSi lock-in pixel with various pixel design splits and at different wavelengths.

To investigate the feasibility of GeSi lock-in pixel pitch scaling, we design a series of GeSi lock-in pixels where their pitches are scaled from 10 µm to 7 µm to 5 µm. Performance parameters such as pixel dark current (I_d), external quantum efficiency (η_q), DC demodulation contrast (C_{dc}), and AC demodulation contrast (C_{ac}) are characterized. Subsequently, a 640×480 VGA resolution GeSi lock-in pixel array in BSI configuration based on a 5 µm pitch device is fabricated and bonded to an application-specific integrated circuit (ASIC) wafer. Point cloud image and depth image are accordingly measured at 940 nm NIR wavelength and 1310 nm SWIR wavelength. In the following sections, we will describe the fabrication and the characterization of these devices.

II. Device Fabrication

Cross-sectional schematic of the GeSi lock-in pixel in BSI configuration is shown in Fig. 1. The front-end processes form a GeSi mesa embedded in a Si wafer, which reduces the topography and simplifies the back-end processes that follow. A series of dopants are implanted and activated, followed by contact formation and metallization. The Si wafer is then bonded to a carrier ASIC wafer with in-pixel connection and polished for back-side processing including backside metal pad opening. Finally, polymer micro-lens (ML) array based on re-flow and etch-back techniques is fabricated on top of the bonded wafer pairs to increase the fill factor of the GeSi lock-in pixel.

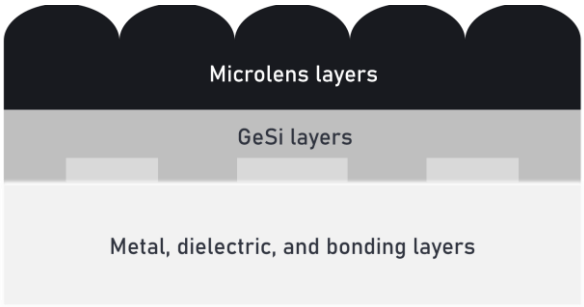

Fig. 1. Cross-sectional schematic of a GeSi lock-in pixel in BSI configuration with polymer ML array on top.

III. Device Characterization

The unit cell pixel pitch is scaled from our previous 10 µm work [4] to 7 µm and 5 µm, and the array size is increased from our previous 240×180 HQVGA resolution work [5] to 640×480 VGA. The performance parameters of the scaled GeSi lock-in pixel are compared and plotted in Fig. 2. To briefly summarize, we have achieved about an order of magnitude pixel dark current reduction as shown in Fig. 2(a), but maintaining similar external quantum efficiency and slightly smaller DC/AC demodulation contrasts as shown in Fig.2(b)-(d). The external quantum efficiency in Fig. 2(b) is measured at 940 nm wavelength, and the slightly different values at different pixel pitches are mainly due to the fact that the polymer ML is individually optimized for each pixel pitch given different camera optics condition. Note that for 640×480 VGA resolution application, the 5 µm pixel design focuses on achieving a lower pixel array power consumption and thus we design the 5 µm pixel with late sublinear switching behavior compared to the 10 µm pixel design, causing slightly lower DC demodulation contrasts as shown in Fig. 2(c). Fig. 2(d) shows the correlation between the DC demodulation contrast and the AC demodulation contrast at 300 MHz modulation frequency for various 5 µm and 7 µm pitch pixel design splits. It can be observed that the correlation between DC and AC demodulation contrasts is clearly positive but at different strengths for 7 µm and 5 µm pitch pixels. Note that similar to DC demodulation contract, we choose 5 µm pitch design with slightly lower AC demodulation contrast compared to 10 µm pitch designs for 640×480 VGA resolution application to achieve a lower pixel array power consumption.

Finally, Table 1 summarizes the performance of 10 µm and 5 µm pitch GeSi lock-in pixels for comparison purpose.

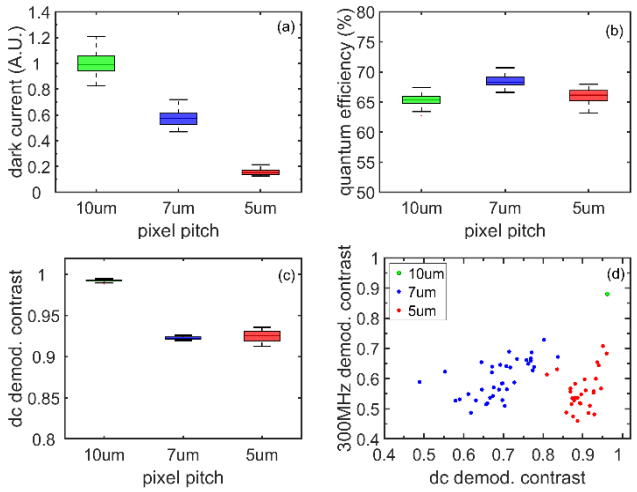

Fig. 2. Pixel (a) I_d (b) η_q (c) C_{dc} scaling with pixel pitch. (d) 300 MHz C_{ac} and C_{dc} correlation with pixel pitches. All measurements are done at 940 nm wavelength.

TABLE I. GESI LOCK-IN PIXEL PERFORMANCE SUMMARY

Pitch	**10µm ([5,6])**	**5 µm (this work)**
Array Size	240×180 HQVGA	640x480 VGA
I_d	100%	16%
ML Fill Factor	~90%	>95%
η_q @ 940 nm	66%	67%
η_q @ 1310 nm	61%	60%
C_{dc}	0.99	0.90
C_{ac} @ 300MHz	0.8	0.7

IV. SYSTEM EVALUATION

We set up two close-range 3D imaging modules to demonstrate that the 640×480 VGA resolution pixel array is capable of detecting NIR and SWIR wavelengths, respectively. In Fig. 3, we capture the NIR point cloud image of a sculpture of David's head under 940 nm wavelength illumination. Due to the high resolution of a 640×480 VGA pixel array, very fine details can be clearly distinguished in real-time. In Fig. 4, we capture the RGB image and the SWIR depth image under 1310 nm wavelength illumination of an 8-inch Si wafer in front of several candles. We can clearly identify the candles behind the Si wafer under 1310 nm wavelength illumination although they are visually blocked by the Si wafer. Note that in the depth image the green/yellow color on the 8-inch Si wafer surface is an artifact due to the multi-path interference between the specular surfaces of the 8-in Si wafer and the test board of the close-range 3D imaging module, and can be further minimized by compacting the test board size.

V. SUMMARY

Here we demonstrate GeSi lock-in pixels with pitches scaled from 10 µm, 7 µm, to 5 µm. Their performance parameters are characterized and we choose 5 µm pitch device to form a 640×480 VGA resolution GeSi lock-in pixel array in BSI configuration bonded to an ASIC wafer. Point cloud image and depth image respectively obtained at 940 nm and 1310 nm wavelengths are presented, paving the route to SWIR 2D/3D imagers on CMOS image sensor compatible platform as well as possible adoption of SWIR eye-safe lasers.

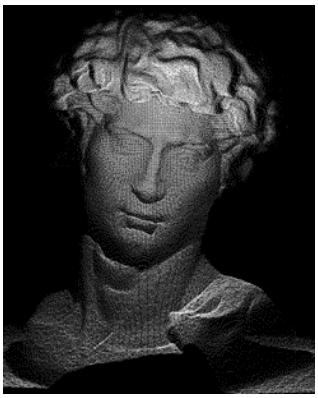

Fig. 3. 640×480 VGA point cloud image of a sculpture of David's head under 940 nm wavelength illumination.

Fig. 4. RGB image (left) and depth image under 1310 nm wavelength illumination (right).

ACKNOWLEDGMENT

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