Integrated SWIR Single-Photon Receiver for Quantum and Bio Photonics Applications (*Invited*)

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Abstract: An integrated shortwave infrared (SWIR) single-photon receiver (SPR), consisting of germanium-silicon (GeSi) single-photon avalanche diode (SPAD)-based pixels bonded to time-to-analog converter (TAC)-based readout integrated circuits (ROICs), is presented in this paper. Compared to the conventional time-to-digital converter (TDC)-based ROICs, our approach provides a high timing resolution without resorting to advanced CMOS technology nodes, and solves the resource conflicts due to TDC sharing.

1. Introduction

The germanium-silicon (GeSi) single-photon avalanche diode (SPAD), due to its compatibility with CMOS fabrication and integration, has long been considered a powerful detection technology for shortwave infrared (SWIR) sensing and imaging. However, its utilization has also long been limited to lab equipment because a cryogenic operation temperature is typically required to suppress the high dark count rate (DCR). Such a situation has changed since the first demonstration of room temperature operation of GeSi SPADs [1,2], in which an ultralow dark current density, i.e., about 8 pA from a 15 μm diameter Ge-on-Si layer (see Ref. [3] for more data), is made possible. This opens tremendous opportunities in practical applications, such as eye-safe light LiDAR for autonomous driving and AR/VR. Brief reviews of the technological and historical developments of GeSi detectors toward single-photon level sensitivity can be found in Refs. [4,5].

From the receiver point of view, the performance of a single-photon receiver (SPR) highly depends not only on the SPAD but also on the analog-frontend (AFE). Conventionally, quenching circuits followed by time-to-digital converters (TDCs) are the mainstream choice and have been recently implemented for the GeSi SPAD [1,6,7]. However, despite the success of TDC, since its high timing resolution is digitally implemented, an advanced CMOS technology node is needed which significantly drives up the cost. More importantly, due to its larger size compared to a single pixel, a row or a column of pixels is often shared so that a spatial "pile-up" event would spoil the acquisition of the spatial correlation. Such an issue makes the AFE consisting of the TDC array not best suitable for certain application, e.g., 1) measurement-based photonic quantum computing (MBPQC), in which faithful detections of the presence of all single photons arriving at the SPAD array are the key to the successful formation of cluster states [8], and 2) fluorescence lifetime imaging microscopy (FLIM), in which faithful detections of the time-of-flight (TOF) information of the first photons arriving at the SPAD array are the key to the fast acquisition of fluorescence lifetime [9]. In this paper, we introduce a novel time-to-analog converter (TAC) to solve the issues as mentioned above, in which the spatial diversity of the presence and the TOF information captured by the SPAD array can be maximized using only a submicron CMOS technology node.

2. Architecture, design, and results

The ROICs are designed for a 2 × 244 SPAD array with per-pixel quenching and TAC circuit, as shown in the left of Fig. 1. The SPAD array is die-bonded to the ROIC chip, and every SPAD pixel is enabled for detection within a pre-determined global timing window, in which all TACs track and hold their unique analog timing information, if any, from the corresponding SPAD pixels. 8-bit 1 Gs/s column-parallel single-slope analog-to-digital converters (SS ADCs) are used for all columns, and all pixels in the same column can be read out sequentially through these SS ADCs. A double-sampling scheme is available in these ADCs to enable the fixed-pattern cancellation. The implemented SPR can be controlled through an I^2C interface and the captured data are sent out through GPIO.

Simplified schematics of the TAC and its operation timing are shown in the middle and the right of Fig. 1, respectively. A column ramp generator initiated by the START signal provides a 1.2 V analog slope with 10 ns to 1.3 μs ramp time through a source follower (SF) to every TAC, depending on the expected range of TOF. Once the

corresponding SPAD is triggered, an analog voltage V_{TAC} is stored on the capacitor C_{TAC} through a track-and-hold circuit. The column readout is then performed by enabling the row-select switch right after the operation of the ramp generator. By minimizing the ramp time of the ramp generator, the TAC features a timing resolution down to 39 ps. Compared to the conventional TDC [10-11] using a deep submicron CMOS technology node, the novel TAC showcases an even finer resolution using only a standard 0.13 µm CMOS technology node. Furthermore, there are no TDC resource conflicts because all the analog timing information can be individually retained on the per-pixel capacitors during the readout time, enabling the capture of the complete spatial correlation from the incoming photons. Consequently, the novel TAC can be beneficial to certain quantum and bio photonics applications.

The measured histogram of the proposed ROIC is shown in the left of Fig. 2. A laser pulse with a fixed delay relative to the START signal is applied to the SPAD array repeatedly, and the captured data are processed by an external FPGA. Clear peaks and their time bins can be found without any numerical algorithm. The measured linearity of the TAC is shown in the right of Fig. 2. Due to the body effect of the SF, the linearity is limited but is relatively constant during the TOF. Note that a simple foreground calibration can be applied to remove the non-idealities. The measured equivalent rms jitter of the TAC plus the column SS ADC is 40 ps.

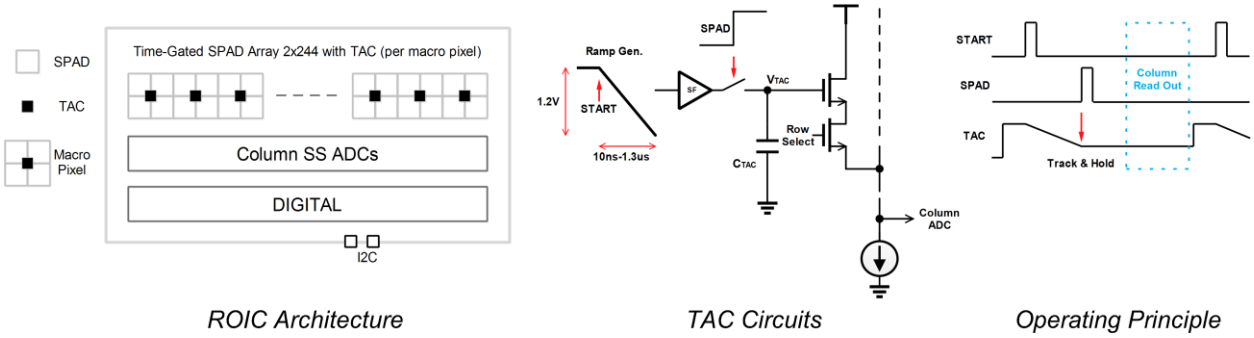

Fig. 1. ROIC architecture and TAC design.

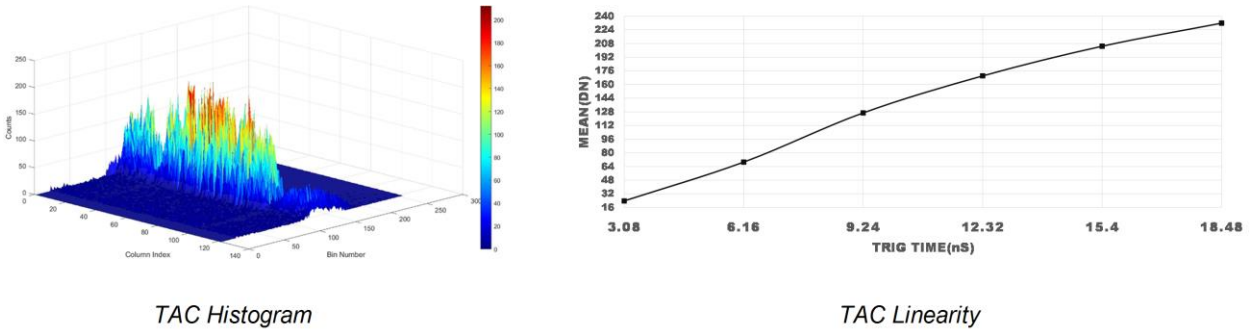

Fig. 2. Measurement results.

3. References

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