

High-Performance Germanium-on-Silicon Lock-in Pixels for Indirect Time-of-Flight Applications

N. Na*, S.-L. Cheng, H.-D. Liu, M.-J. Yang, C.-Y. Chen, H.-W. Chen, Y.-T. Chou, C.-T. Lin, W.-H. Liu, C.-F. Liang, C.-L. Chen, S.-W. Chu, B.-J. Chen, Y.-F. Lyu, and S.-L. Chen
Artilux Inc., Zhubei City, Hsinchu County, Taiwan ROC
* Email: rp@artiluxtech.com

Abstract—We investigate and demonstrate the first Ge-on-Si lock-in pixels for indirect time-of-flight measurements. Compared to conventional Si lock-in pixels, such novel Ge-on-Si lock-in pixels simultaneously maintain a high quantum efficiency and a high demodulation contrast at a higher operation frequency, which enable consistently superior depth accuracies for both indoor and outdoor scenarios. System performances are evaluated, and pixel quantum efficiencies are measured to be $>85\%$ and $>46\%$ at 940nm and 1550nm wavelengths, respectively, along with demodulation contrasts measured to be >0.81 at 300MHz. Our work may open up new routes to high-performance indirect time-of-flight sensors and imagers, as well as potential adoptions of eye-safe lasers (e.g. wavelengths $>1.4\mu\text{m}$) for consumer electronics and photonics.

I. INTRODUCTION

1D depth sensors and 3D image sensors are vital to a variety of applications such as hand tracking, facial recognition, 3D model scanning, simultaneous localization and mapping for spatial navigations, surveillance, and light detection and ranging for autonomous vehicles, to name a few. There are at least four major techniques that are well studied in the literature, i.e., passive/active stereovision [1], structured light imaging [2], direct time-of-flight (TOF) sensing via single photon avalanche photodiodes and time-to-digital converters [3], and indirect TOF sensing via lock-in pixels [4]. In particular, the indirect TOF measurement features advantages such as direct acquisition of a depth information without additional computational algorithms, simple laser light projector without complex optical modules, and low power consumption with respect to pixel size/number scaling.

The principle of the indirect TOF measurement is essentially based on homodyne detection with radio-wave operation frequency f_o , in which the roles of a local oscillator/mixer/detector are replaced by a single lock-in pixel, to demodulate the transmitted laser light that is initially modulated at f_o , then reflected from a 3D object, and finally received by the lock-in pixel. Various Si lock-in pixels have been proposed and demonstrated, such as one-tap CCD [5], demodulated photogates [6], pinned photodiode with transfer gates [7], and current assisted photonic demodulator [8]. To achieve a high signal-to-noise ratio and hence a small depth error in an indirect TOF system, it is desired to increase the pixel quantum efficiency η_q and frequency bandwidth B_f . However, especially with the recent trend to shift the laser wavelength from 850nm to 940nm to take advantage of the

solar ambient spectrum dip at 940nm, η_q degrades further as Si features a weaker absorption at a longer wavelength. Limited by the efficiency-bandwidth-product, while it is possible to obtain a higher η_q by simply having a thicker Si absorption layer, the resultant smaller B_f may in return spoil the depth accuracy. Consequently, it has become very challenging to engineer a high-performance Si lock-in pixel.

In this paper, we present novel Ge-on-Si (GOS) lock-in pixels in a two-tap configuration as shown in Fig. 1, at 940nm (for indoor-to-outdoor applications) and 1550nm (for eye-safe applications) wavelengths. Due to the $\sim 0.8\text{eV}$ direct bandgap of Ge, compared to Si, a stronger absorption manifests itself with cut-off wavelength up to $1.6\mu\text{m}$ wavelength [9]. Such a property boosts the pixel η_q and B_f , and reduces the depth error measured in an indirect TOF system. Moreover, our GOS lock-in pixels are developed via Taiwan Semiconductor Manufacture Company (TSMC) image sensor platform, demonstrating the technology can be incorporated into the manufacture of FSI/BSI CMOS image sensors.

II. EVALUATION OF SYSTEM PERFORMANCES

We first calculate and compare the depth errors of a Si pixel and a GOS pixel at 940nm. The parameters used are listed in Table 1, and their values are based on Ref. [10-11] and Ref. [12] for Si and GOS, respectively. In Fig. 2, we plot depth errors of the Si and GOS pixels as a function of depth, for both the indoor and outdoor cases, given the laser power equal to 2W. It is observed that, for the indoor case, the depth error of the GOS pixel is about the same as or better than that of the Si pixel; moreover, for the outdoor case, the depth error of the GOS pixel is significantly better than that of the Si pixel (for more details please see Ref. [13]). These results might be surprising at the first sight as the dark current I_d of the GOS pixel is set to be orders of magnitude larger than that of the Si pixel (the depth errors in Fig. 2 remain almost the same even if a lower Si pixel I_d is used). The reason lies on that, in an indirect TOF system, the dominant noise factor is in fact due to the indoor/outdoor ambient light and laser light for the given indoor/outdoor scenarios. This is in sharp contrast to the earlier efforts in replacing InGaAs with GOS to make SWIR sensors, in which the system noise is limited by pixel I_d because the application mainly emphasizes on weak light detection, but analogous to the recent efforts in replacing III-V compound semiconductors with GOS to make high-speed optical receivers [9], in which the system noise is limited by the input referred noise of a transimpedance amplifier instead of detector I_d .

III. CHARACTERIZATION OF DEVICE PROPERTIES

The GOS lock-in pixels are fabricated in a BSI configuration and characterized on a wafer-level electrical-optical tester for various dc/ac parameters. In Fig. 3, we show the measured I_d at V_2 node from 4 different lots. One wafer is selected from each lot, in which Lot1 is prepared via a first design/process vehicle, and Lot2~Lot4 are prepared via a second design/process vehicle. The same pixel is measured over 37 dies with at least 3 repeats for each wafer. Except for a few outliers, it is observed that for each lot I_d features a tight distribution and is significantly improved by almost two orders of magnitudes from Lot1 to Lot2~Lot4, because of improved designs and Ge processes. Note that I_d in Lot2~Lot4 is consistent with the assumed I_d used in generating Fig. 2. In Fig. 4, the external η_q is measured and steadily improved from Lot2 to Lot4 up to ~85% (median value with $\pm 5\%$ measurement error), because of further design and Ge process optimizations. In Fig. 5, we prepare a scatter plot to correlate the measured I_d and η_q , in which the improvements from the 1st to the 2nd vehicle can be clearly seen. In Fig. 6 and 7, we plot I_d as a function of V_2 and ΔV , respectively. The apparent increase of I_d with V_2 is caused by the increased local electric field and so the corresponding carrier generation rate. Nevertheless, I_d changes little with ΔV as the switching region is distant from V_2 node. In Fig. 8 and 9, we plot η_q as a function of V_2 and ΔV , respectively. η_q slightly increases with both V_2 and ΔV because of a faster carrier transit time that reduces the chance of carrier recombination. Note that from Fig. 6 to 9, 2~3 dies with 60 repeats are measured for each wafer.

In Fig. 10, we show the measured average power P_a from 3 different lots. Two distinct device groups M and N are presented, in which group M features standard designs and group N features low-power designs. It can be seen that an effective ~5 times reduction is achieved in Lot2/Lot3. In Fig. 11, the dc demodulation contrast C_{dc} is measured from 3 different lots. It can be seen that C_{dc} in group M is slightly higher than that of group N in Lot2/Lot3, suggesting a trade-off between P_a and C_{dc} . This is further evidenced by the correlation shown in Fig. 12 scatter plot. Note that from Fig. 10 to 12, the low-power devices in Lot4 are designed to be less aggressive compared to Lot2/Lot3, and experimentally shown to feature a less clear P_a -to- C_{dc} trade-off. In Fig. 13 and 14, C_{dc} are plotted as a function of V_2 and ΔV , respectively, with only group M shown for simplicity. C_{dc} changes very little with V_2 as the switching region is distant from V_2 node. On the other hand, C_{dc} increases with ΔV in a linear/sublinear fashion between 0V~0.2V/0.2V~0.8V, and saturates beyond 0.8V, showing a good two-tap switching capability. Note that in Fig. 14 the slightly lower C_{dc} in Lot3 is analyzed and found to be induced by wafer-to-wafer process variation.

In Fig. 15 and 16, given 940nm/1550nm wavelengths and Lot1/Lot2 wafers, we present scatter plots between I_d and η_q for group M and N, respectively, over 37 dies with at least 3 repeats for each wafer. The spreads of experimental data mainly arise from including >2 pixel designs to investigate the wavelength sensitivity. It can be seen that the highest η_q at 1550nm is ~50%, suggesting a large tensile-strain enhanced

Ge absorption [9]. From Fig. 17 to 20, scatter plots between P_a and C_{dc} are presented for group M and N, with the wafers of Lot1/Lot2 and the wavelengths of 940nm/1550nm, over 2~3 dies with at least 3 repeats for each wafer. The spreads of experimental data mainly arise from including >600 designs to cover a large design space. Similar distributions between the scatter plots at 940nm or 1550nm for the same pixel are observed, suggesting the dissimilar spatial carrier distributions (exponential at 940nm and nearly constant at 1550nm) caused by different absorption coefficients has a minimum impact. Moreover, C_{dc} is improved from the 1st to the 2nd vehicle, i.e., from Lot1 to Lot2, and again P_a is reduced from group M to N. Note that the long red tails in Fig. 19 and 20 suggest that there is a limit to the low-power design rendering switching capability degradation. In Fig. 21 and 22, scatter plots between P_a and ac demodulation contrast C_{ac} are presented for group M and N in Lot2, at 940nm and 1550nm, respectively. The trade-off between P_a and C_{ac} are observed, as in P_a and C_{dc} . Further evidence is provided in Fig. 23 using Lot4 data at 940nm, as C_{dc} and C_{ac} up to 0.97 and 0.83 show a positive correlation.

IV. SUMMARY

Novel GOS lock-in pixel is investigated at 940nm and 1550nm wavelengths and shown to be a strong contender against conventional Si lock-in pixel. The measured statistical data further demonstrate the technology yields good within-wafer and wafer-to-wafer uniformities that may be ready for mass production in the near future.

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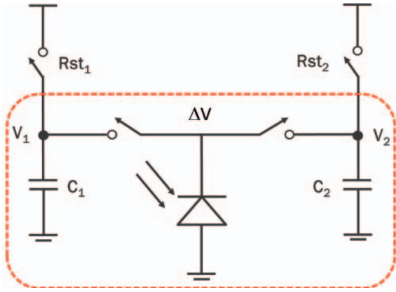


Fig. 1 The equivalent circuit of a two-tap lock-in pixel. Differential voltage ΔV is applied to control the two demodulation switches; voltages V_1/V_2 are applied to extract the photo-carriers.

Table 1 System parameters		
Pixel Type	Si	Ge-on-Si
Laser Wavelength	940 nm	
Pixel Pitch	10 μm	
Camera Effective Focal Length	2 mm	
Camera Focal Number	1.1	
Absorption Efficiency	20 %	90 %
Operation Frequency	100 MHz	300 MHz
Demodulation Contrast at Operation Frequency	0.85	0.9
Effective Bandpass Filter Linewidth	60 nm	
Indoor & Outdoor Ambient Light Spectral Intensity	3 & 300 $\text{mW}/\text{m}^2/\text{nm}$	

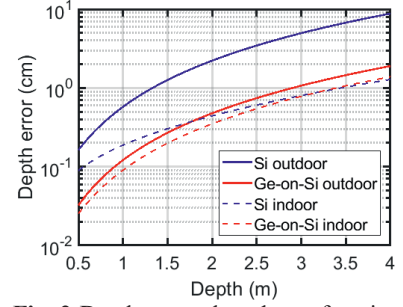


Fig. 2 Depth error plotted as a function of depth for Si and GOS lock-in pixels at indoor/outdoor ambient conditions.

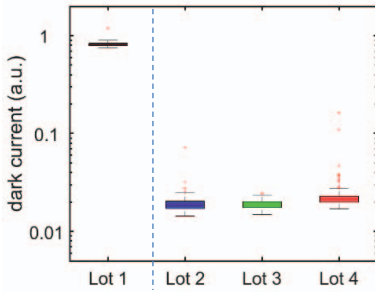


Fig. 3 I_d plotted with 4 different lots; Lot1 is from the 1st vehicle and Lot2~Lot4 are from the improved 2nd vehicle with I_d reduced by roughly 2 orders of magnitude.

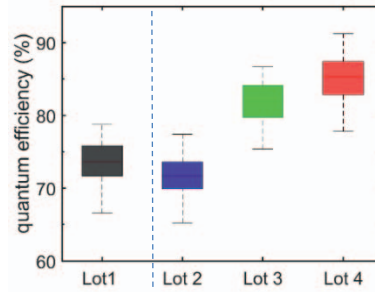


Fig. 4 η_q plotted with 4 different lots; Lot1 is from the 1st vehicle and Lot2~Lot4 are from the improved 2nd vehicle with η_q gradually improved by design/process optimizations.

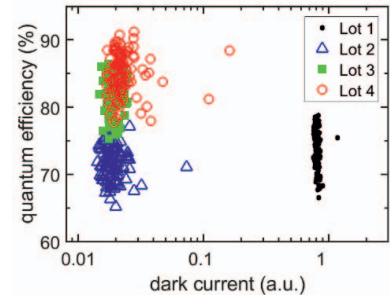


Fig. 5 η_q plotted as a function of I_d with 4 different lots.

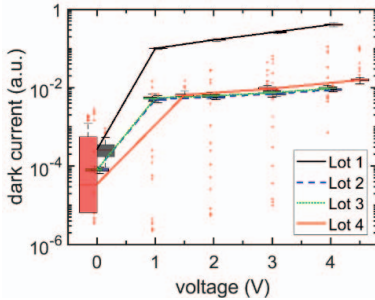


Fig. 6 I_d plotted as a function of V_2 . Lines intercepting median values are drawn for visual comparison.

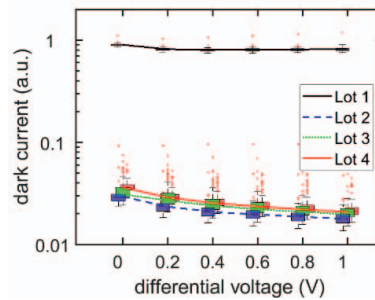


Fig. 7 I_d plotted as a function of ΔV . Lines intercepting median values are drawn for visual comparison.

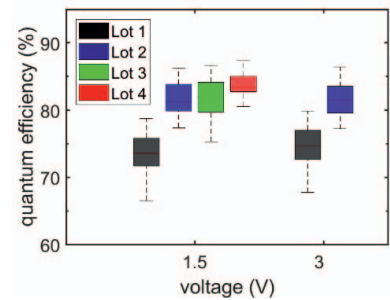


Fig. 8 η_q plotted as a function of V_2 . Only data at 1.5V and 3V are shown.

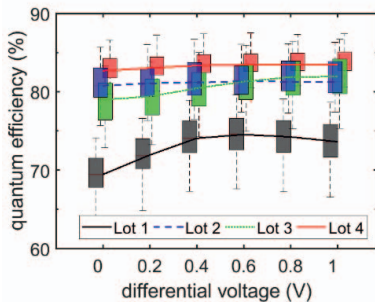


Fig. 9 η_q plotted as a function of ΔV . Lines intercepting median values are drawn for visual comparison.

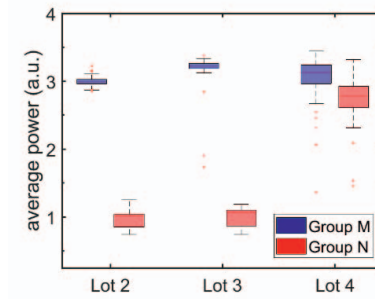


Fig. 10 P_a plotted with 3 different lots for group M/N standard/low-power designs. Note that the low-power designs in Lot4 are less aggressive.

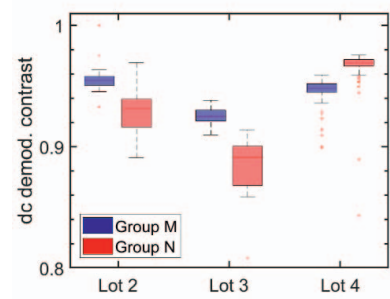


Fig. 11 C_{dc} plotted with 3 different lots for group M/N standard/low-power designs. Note that the low-power designs in Lot4 are less aggressive.

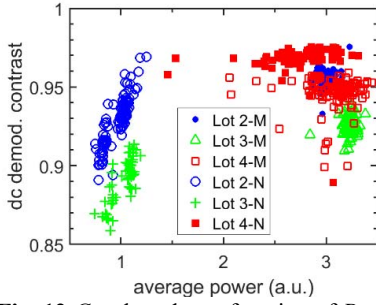


Fig. 12 C_{dc} plotted as a function of P_a . Note that the low-power designs in Lot4 are less aggressive.

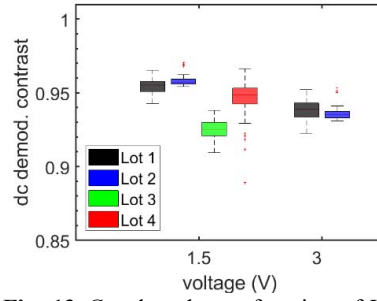


Fig. 13 C_{dc} plotted as a function of V_2 for group M standard design. Only data at 1.5V and 3V are shown.

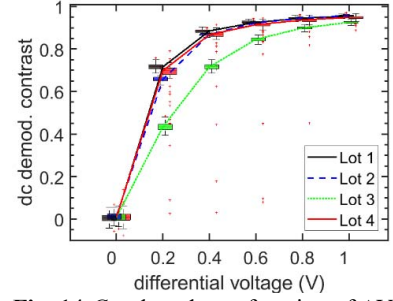


Fig. 14 C_{dc} plotted as a function of ΔV for group M standard design. Lines intercepting median values are drawn for visual comparison.

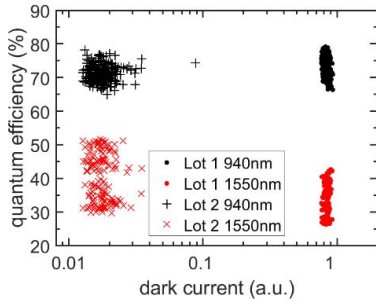


Fig. 15 η_q plotted as a function of I_d for group M standard design. Note that the 940nm data are selected from Lot1/Lot2 for visual comparison rather than the highest η_q .

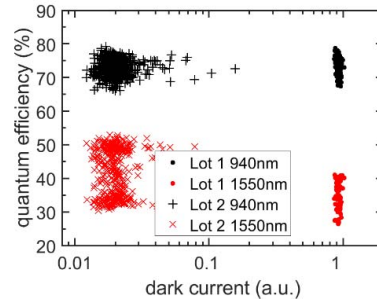


Fig. 16 η_q plotted as a function of I_d for group N low-power design. Note that the 940nm data are selected from Lot1/Lot2 for comparison rather than the highest η_q .

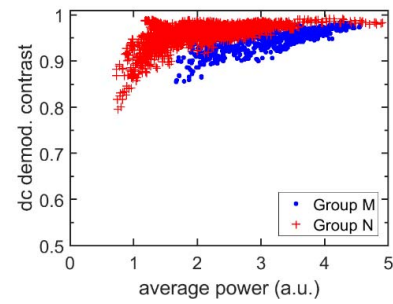


Fig. 17 C_{dc} plotted as a function of P_a for Lot1 with >600 designs at 940nm to cover a large design space.

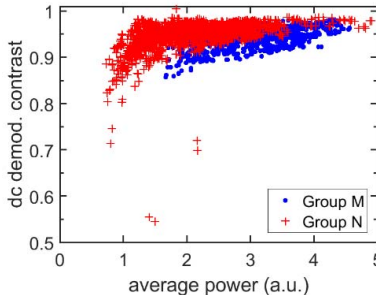


Fig. 18 C_{dc} plotted as a function of P_a for Lot1 with >600 designs at 1550nm to cover a large design space.

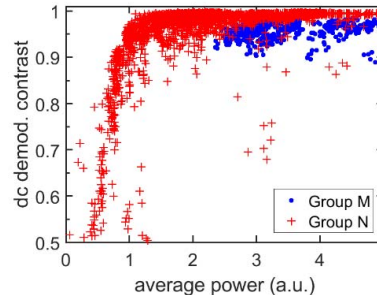


Fig. 19 C_{dc} plotted as a function of P_a for Lot2 with >600 designs at 940nm to cover a large design space.

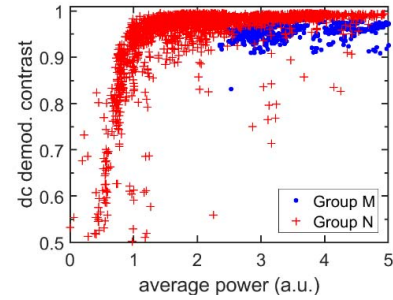


Fig. 20 C_{dc} plotted as a function of P_a for Lot2 with >600 designs at 1550nm to cover a large design space.

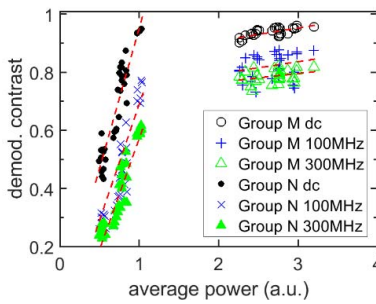


Fig. 21 C_{dc} and C_{ac} plotted as a function of P_a for Lot2 at 940nm. Note that compared to Lot4, the low-power designs in Lot2 are more aggressive.

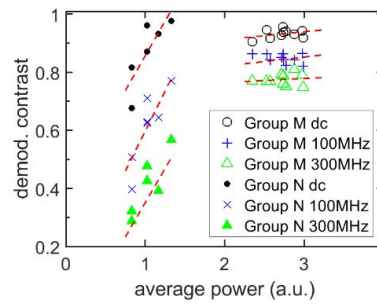


Fig. 22 C_{dc} and C_{ac} plotted as a function of P_a for Lot2 at 1550nm. Note that compared to Lot4, the low-power designs in Lot2 are more aggressive.

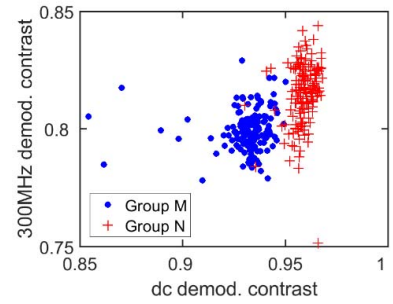


Fig. 23 300MHz C_{ac} plotted as a function of C_{dc} for Lot4 at 940nm. Note that compared to Lot2, the low-power designs in Lot4 are less aggressive.